## IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

*Listing of Claims*

1 - 5. (Canceled)

6. **(Currently Amended)** ~~A device according to claim 5,~~ A device for data stream analyzing, comprising:

a processor means, a program memory, and a multiplexable data stream delayline for receiving a data stream; said device for enabling parsing of said data stream in a way that is controlled by an interchangeable program; and

a multiplexing means for connecting different parts of said data stream to said processor means, wherein the multiplexing means include a multiplexing control means for automatically keeping track of where specific data is located in the delayline and for enabling at least one program to start executing once the data is received in the delayline;

wherein the multiplexing control means automatically keeps track of where specific data is located in the delayline by the use of a first and second position register that change in a predetermined way when a packet is forwarded in the delayline, and

wherein values of the position registers are changed in the following way: when a packet arrives, the first register starts to increment for every byte; when the packet has come to its end, where the packets DV (data valid) signal becomes false again, the first register stops counting and the second register starts to increment.

7. (Previously presented) A device for data stream analyzing comprising a processor means, a program memory, and a multiplexable data stream delayline for receiving a data stream, said device for enabling parsing of said data stream in a way that is controlled by an interchangeable program; further comprising a multiplexing means for connecting different parts of said data

stream to said processor means; wherein the multiplexing means includes a multiplexing control means for automatically keeping track of where specific data is located in the delayline and for enabling at least one program to start executing once the data is received in the delayline; wherein the multiplexing control means automatically keeps track of where specific data is located in the delayline by the use of a first and second position register that change in a predetermined way when a packet is forwarded in the delayline; and wherein said device automatically keeps track of where specific data is located in the delayline, by the use of said dedicated position registers together with the use of a formula

P = tagfield + lastfield – wanted_tag

and "P" is the position of a wanted byte in the delayline; "tagfield" is the value of the first register; "lastfield" is the value of the second register and "wanted_tag" is the position of a wanted byte relative to the beginning of the packet

8 - 11. (Canceled)